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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,727	03/08/2004	Jeffrey R. Jobs	33585/US	3937

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EXAMINER	
PATEL, HETUL B	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 09/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/797,727	JOBS ET AL.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-122* is/are pending in the application.

4a) Of the above claim(s) 2, 18, 45, 48 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

PB 6)☒ Claim(s) ~~*1-122* is/are rejected~~. 1, 3-17, 19-44, 46-47, and 49-122 are rejected

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06/26/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to communication filed on June 26, 2006. This amendment has been entered and carefully considered. Claims 2, 18, 45 and 48 are cancelled; claims 1, 17, 36 and 47 are amended; and claims 58-122 are newly added. Therefore, claims 1, 3-17, 19-44, 46-47 and 49-122 are pending in the current application.

2. The indicated allowability of claims 2-4, 7-15, 18-20, 23-34, 45-46 and 48-55 in the previous office action is withdrawn and as a result of that, the current office action is made Non-final.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 15, 33, 64, 71, 76, 80, 82-83, 90, 96, 101 and 104 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

According to the specification of this application, the packet includes a command header followed by read or write data (e.g. see paragraph [009] , lines 5+ on page 4). Examiner is puzzled by the phrase "coupling a packet containing command, address and data signals ..." as used in claims 15, 33, 64, 71, 76, 80, 82-83, 90, 96, 101 and 104. It is unclear how to couple a packet containing the command header followed by read or write data with the memory hub.

Claim Objections

4. Claims 49-52 are objected to under 37 CFR 1.75(c), as being of improper dependent form because they depend upon the cancelled claim 48. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3-14, 17, 19-32, 34, 36, 38-44, 47, 49-63, 66-70, 73-75, 78-79, 84-89, 91, 93-95, 97, 99-100, 102, 105, 107 and 118-121 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamilton et al. (Pat No 4443845) and further in view of Krull et al. (Pat No 6301637).

Regarding claims 1, 17, and 36, Hamilton et al. describes a memory system with a method of coupling command, address and data signals between the memory hub controller and the memory hub in the at least one memory module, the method comprising: coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using a communications path having a first capacity; coupling data signals from the memory hub in the at least one memory module to the memory hub controller using a communications path having a second capacity, where the sum of the first capacity and the second capacity is a fixed value; having M buffers, N of the M buffers being configured as output buffers and P of the M buffers being configured as input buffers, at least one memory module, comprising a memory hub having a plurality of buffers, N of which are configured as input buffers and P of which are configured as output buffers; and altering the first capacity and the second capacity during the operation of the memory system based on the rate at which the selected signals are being coupled (i.e. selectively transmitting the selected ones of said command, data and address signals on the bus) (column 1, lines 25-59 and column 11, line 64 to column 13 line 10).

However, Hamilton et al. does not expressly describe having a memory hub and at least one memory module having a memory hub and a plurality of memory devices coupled to the memory hub.

Krull et al. describes having a memory hub and at least one memory module having a memory hub and a plurality of memory devices coupled to the memory hub (column 5, lines 37-52).

Hamilton et al. and Krull et al. are analogous art because they are from the same field of endeavor, memory. At the time of the invention it would have been obvious to a person of ordinary skill in the art to have the memory have a memory hub. The suggestion for doing so would have been for better efficiency with memory. Therefore, it would have been obvious to combine Krull et al. and Hamilton et al. for the benefit of more efficient memory to obtain the invention as specified in claims 1, 17, 36.

Regarding claims 3-8, 10-11, 19-26, 28-29, 34, 38-44, 47 and 49-55, the combination of Hamilton et al. and Krull et al. teaches the claimed invention as described above and furthermore, Hamilton et al. teaches that the act of altering the first capacity and the second capacity comprise determining the rate at which the selected signals are being coupled and then altering the first capacity and the second capacity at the determined rate (i.e. selectively transmitting the selected ones of said command, data and address signals on the bus) (e.g. see Col. 1, lines 34-40).

As per claims 59-60, 67, 85-86, 91, 97, 102, 105, 119-120, see arguments with respect to rejection of claims 10-11, 28-29, 34, 38-44 and 54-55. Claims 59-60, 67, 85-86, 91, 97, 102, 105, 119-120 are also rejected based on the same rationale as the rejection of claims 10-11, 28-29, 34 and 54-55 as they comprise same limitations as claims 10-11, 28-29, 34 and 54-55 as indicated by Applicant in Table 2 on page 32 of Remarks.

Regarding claims 9 and 27, the combination of Hamilton et al. and Krull et al. teaches the claimed invention as described above and furthermore, Krull et al. teaches about configuring buffers in the memory hub controller and in the memory hub of at

least one memory module as either input buffers (i.e. 74 in Fig. 3) or output buffers (i.e. 102 in Fig. 3) (e.g. see Fig. 3).

Regarding claims 12, 30 and 56, the combination of Hamilton et al. and Krull et al. teaches the claimed invention as described above and furthermore, Hamilton et al. teaches that the act of altering the first capacity and the second capacity during the operation of the memory system comprise altering the first capacity and the second capacity within a range of minimum and maximum values for the first capacity and the second capacity respectively (i.e. from at least one bus line to all bus lines of the bus based on the selected ones of said command, data and address signals) (e.g. see Col. 1, lines 34-40).

As per claims 61, 68, 87 and 121, see arguments with respect to rejection of claims 12, 30 and 56. Claims 61, 68, 87 and 121 are also rejected based on the same rationale as the rejection of claims 12, 30 and 56 as they comprise same limitations as claims 12, 30 and 56 as indicated by Applicant in Table 2 on page 32 of Remarks.

Regarding claims 13-14 and 31-32, the combination of Hamilton et al. and Krull et al. teaches the claimed invention as described above and furthermore, Hamilton et al. teaches that the act of altering the first capacity and the second capacity comprise manually altering the first capacity and the second capacity by adjusting at least one electrical connection (e.g. see Col. 13, lines 39-42).

As per claims 62-63, 69-70, 74-75, 79, 88-89, 94-95 and 100, see arguments with respect to rejection of claims 13-14 and 31-32. Claims 62-63, 69-70, 74-75, 79, 88-89, 94-95 and 100 are also rejected based on the same rationale as the rejection of

claims 13-14 and 31-32 as they comprise same limitations as claims 13-14 and 31-32 as indicated by Applicant in Table 2 on page 32 of Remarks.

Regarding claim 47, Hamilton et al. discloses a processor-based system, comprising: a processor having a processor bus; a system controller coupled to the processor bus, the system controller having a peripheral device port; a memory hub controller coupled to the processor bus, the memory hub controller having an output port and an input port; a downstream bus coupled between the output port of the memory controller and the memory hub of the at least one memory module, the downstream bus having a width of M bits, the value of M being variable to adjust that bandwidth of the downstream bus; and an upstream bus coupled between the input port of the memory controller and the memory hub of the at least one memory module, the upstream bus having a width of N bits where N is equal to a fixed value less M, the value of N being variable to adjust that bandwidth of the upstream bus (column 1, lines 25-59 and column 11, line 64 to column 13 line 10).

Hamilton et al. does not expressly describe having a memory hub and at least one memory module having a memory hub and a plurality of memory devices coupled to the memory hub.

Krull et al. describes having a memory hub and at least one memory module having a memory hub and a plurality of memory devices coupled to the memory hub (column 5, lines 37-52).

Furthermore, where claim 47 states at least one input device coupled to the peripheral device port of the system controller (i.e. a keyboard or mouse), at least one

output device coupled to the peripheral device port of the system controller (i.e. a monitor), and at least one data storage device coupled to the peripheral device port of the system controller (i.e. a hard drive), the examiner finds these limitations to be inherent.

Hamilton et al. and Krull et al. are analogous art because they are from the same field of endeavor, memory. At the time of the invention it would have been obvious to a person of ordinary skill in the art to have the memory have a memory hub. The suggestion for doing so would have been for better efficiency with memory. Therefore, it would have been obvious to combine Krull et al. and Hamilton et al. for the benefit of more efficient memory to obtain the invention as specified in claims 1, 17, 36.

As per claims 58, 66, 73, 78, 82, 84, 93, 99, 104, 107 and 118, see arguments with respect to rejection of claims 1, 9-10, 12-13, 15, 17, 27, 30-31, 33-34, 47 and 53. Claims 58, 66, 73, 78, 82, 84, 93, 99, 104, 107 and 118 are also rejected based on the same rationale as the rejection of claims 1, 9-10, 12-13, 15, 17, 27, 30-31, 33-34, 47 and 53 as they comprise same limitations as claims 1, 9-10, 12-13, 15, 17, 27, 30-31, 33-34, 47 and 53 as indicated by Applicant in Table 1 on page 31 of Remarks.

6. Claims 16, 35, 37, 46, 57, 65, 72, 77, 81, 92, 98, 103, 106, 108-117 and 122 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamilton et al. and Krull et al. as applied to claims 1, 17, and 47 above, and further in view of Story et al. (Pat No 6434654).

Hamilton et al. and Krull et al. describe all of the limitations of claims 1, 17, and 47, but do not teach the acts of altering the first capacity and the second capacity during the operation of the memory system comprise altering the first capacity and the second capacity during the initialization of the memory system.

Story et al. does teach the acts of altering the first capacity and the second capacity during the operation of the memory system comprise altering the first capacity and the second capacity during the initialization of the memory system (column 2, lines 30-39).

Hamilton et al., Krull et al. and Story et al. are analogous art because they are from the same field of endeavor, memory. At the time of the invention it would have been obvious to a person of ordinary skill in the art to alter the capacities during initialization. The suggestion for doing so would have been more efficient memory accesses, especially from not having to take the cycles to modify the capacities sometime later. Therefore, it would have been obvious to combine Hamilton et al., Krull et al., and Story et al. for the benefit of efficiency to obtain the invention as specified in claims 16, 35, 37, 46, 57 and 65.

As per claims 65, 72, 77, 81, 92, 98, 103, 106, 108, 110 and 122, see arguments with respect to rejection of claims 16 and 35. Claims 65, 72, 77, 81, 92, 98, 103, 106, 108, 110 and 122 are also rejected based on the same rationale as the rejection of claims 16 and 35 as they comprise same limitations as claims 16 and 35 as indicated by Applicant in Table 2 on page 32 of Remarks.

As per claims 109-117, see arguments with respect to rejection of claims 37-44 and 46. Claims 109-117 are also rejected based on the same rationale as the rejection of claims 37-44 and 46 as they comprise same limitations as claims 37-44 and 46 as indicated by Applicant in Tables 1-2 on page 31-32 of Remarks.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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PIERRE BATAILLE
PRIMARY EXAMINER
9/18/06